US 6,754,207 B1

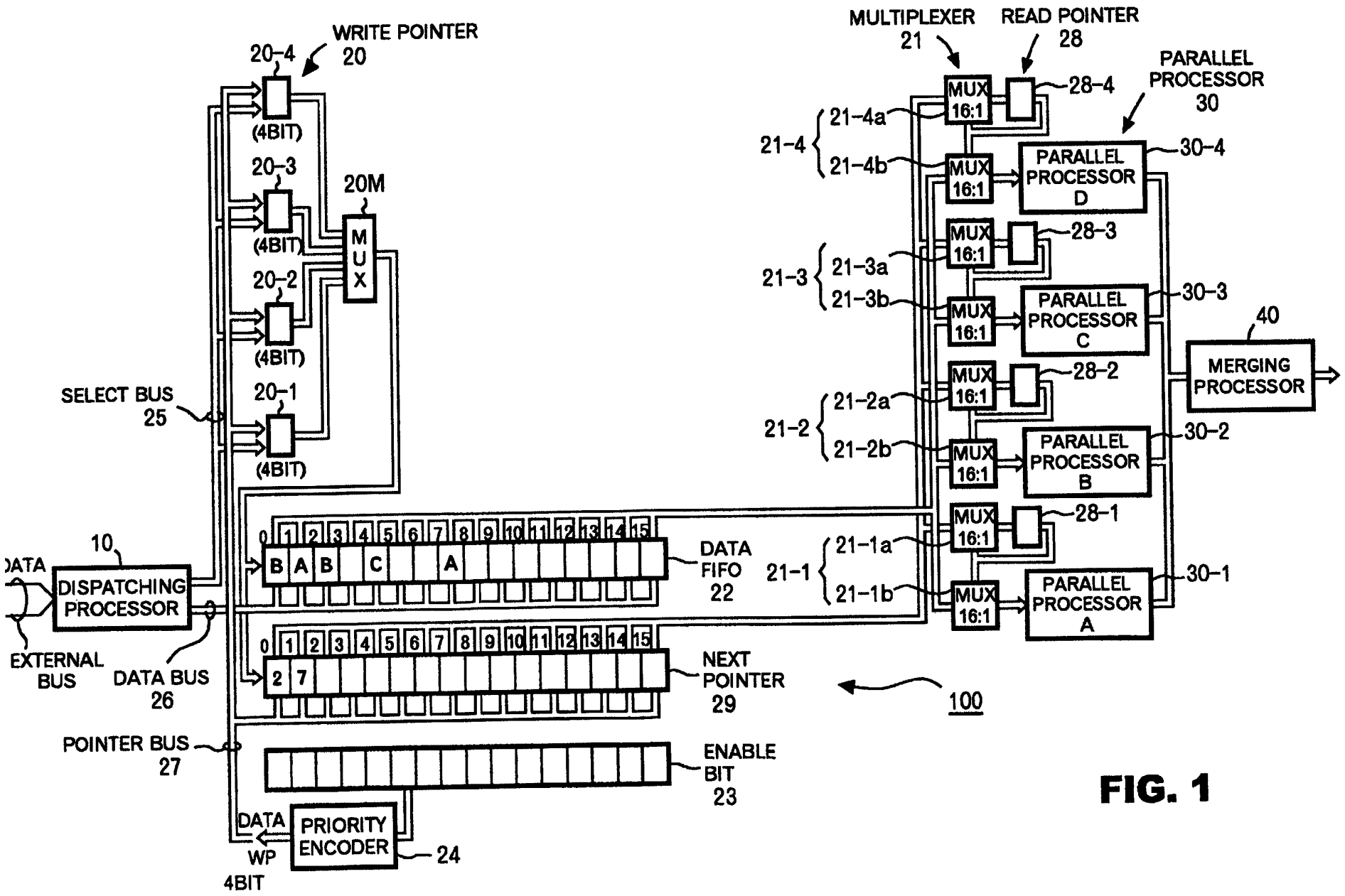

FIG. 1

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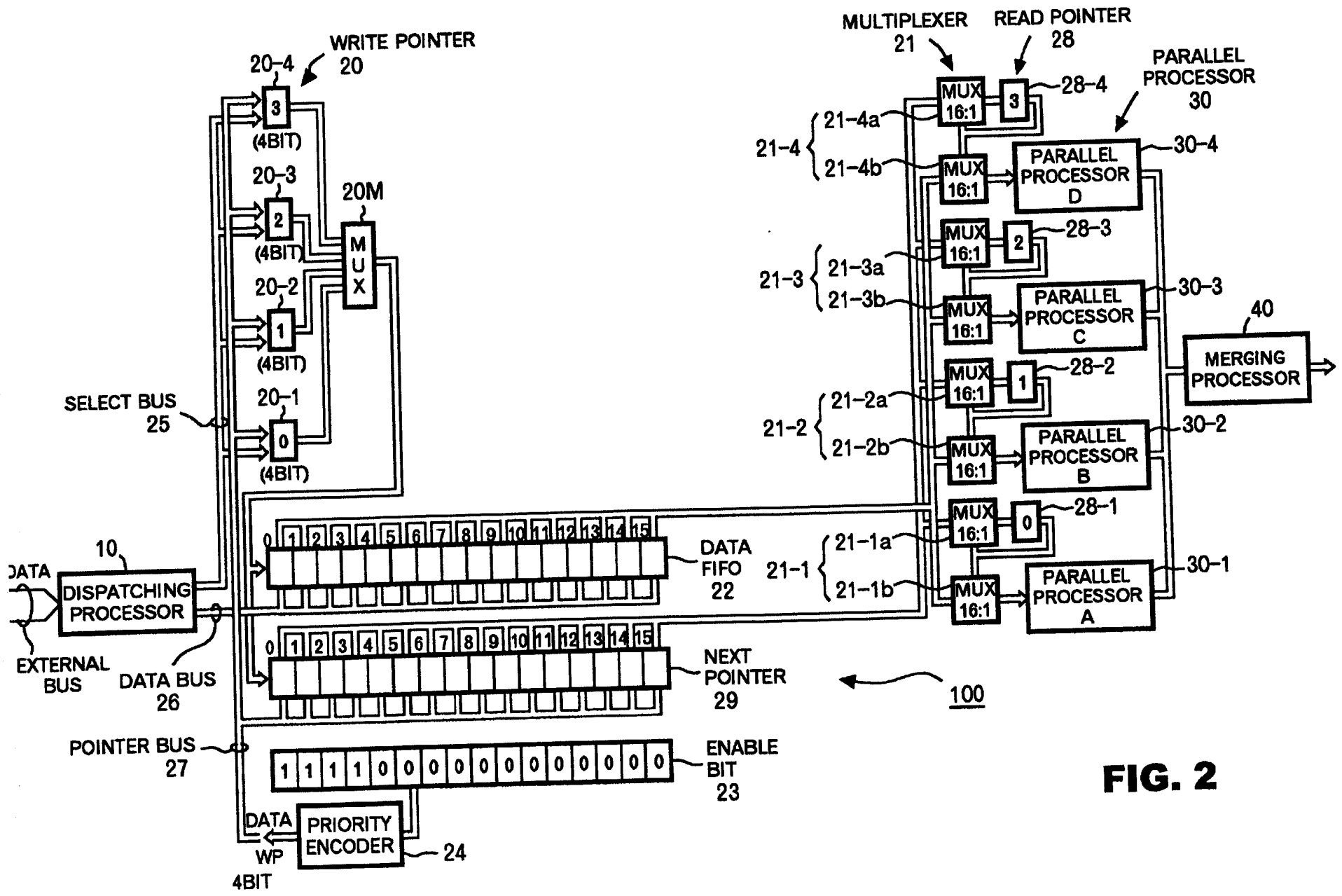

FIG. 2

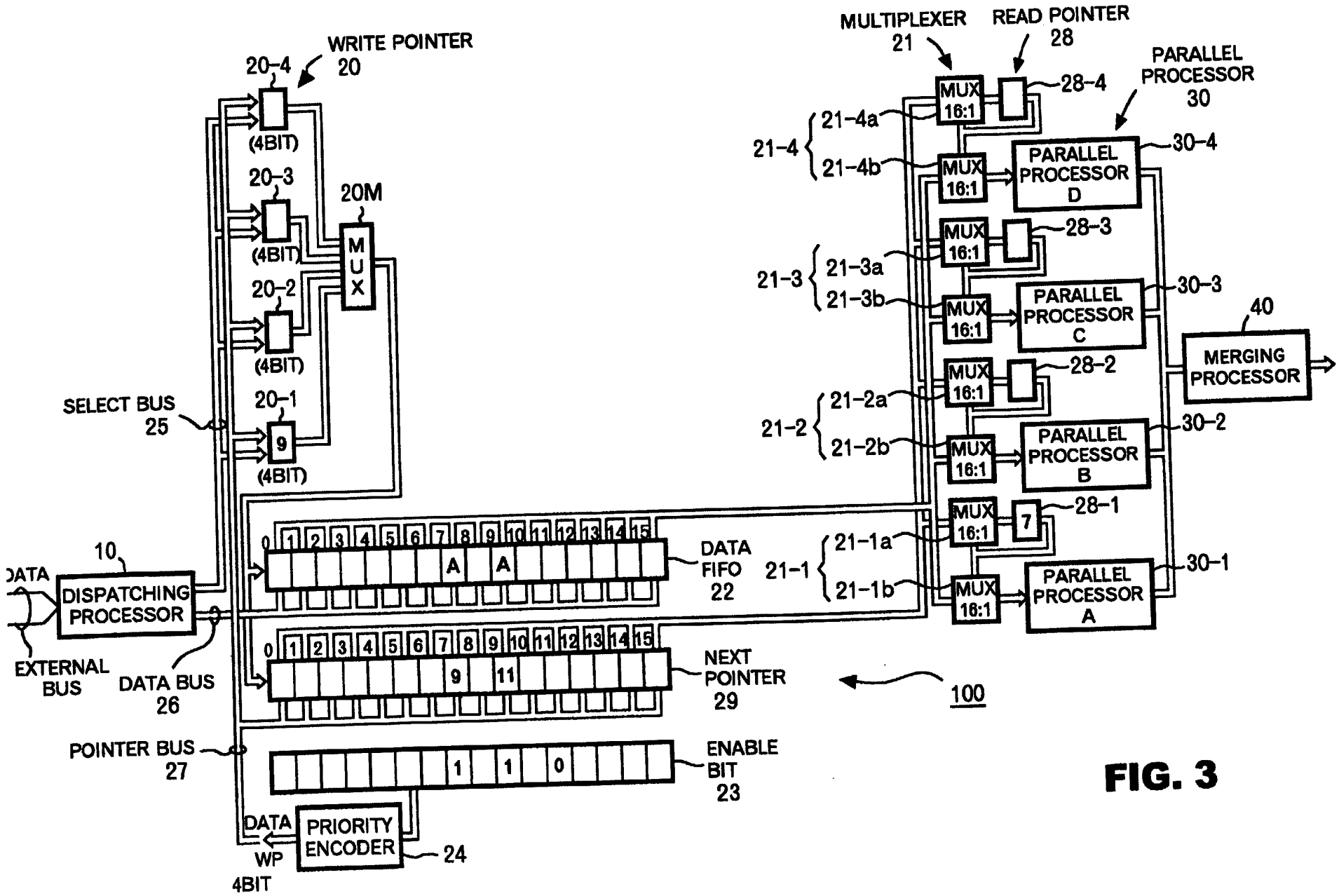
WRITE POINTER
20
20-4
(4BIT)
20-3
(4BIT)
20-2
(4BIT)
20-1
9
(4BIT)
20M
MUX
SELECT BUS
25
10
DISPATCHING PROCESSOR
EXTERNAL BUS
DATA BUS
26
DATA FIFO
22
A
A
NEXT POINTER
29
9
11
POINTER BUS
27
ENABLE BIT
23
1
1
0
DATA
WP
4BIT
PRIORITY ENCODER
24
MULTIPLEXER
21
READ POINTER
28
PARALLEL PROCESSOR
30
MUX 16:1
21-4
21-4a
21-4b
28-4
30-4
PARALLEL PROCESSOR D
21-3
21-3a
21-3b
28-3
30-3
PARALLEL PROCESSOR C
21-2
21-2a
21-2b
28-2
30-2
PARALLEL PROCESSOR B
21-1
21-1a
21-1b
7
28-1
30-1
PARALLEL PROCESSOR A
40
MERGING PROCESSOR
100

FIG. 3

Patent Application Publication

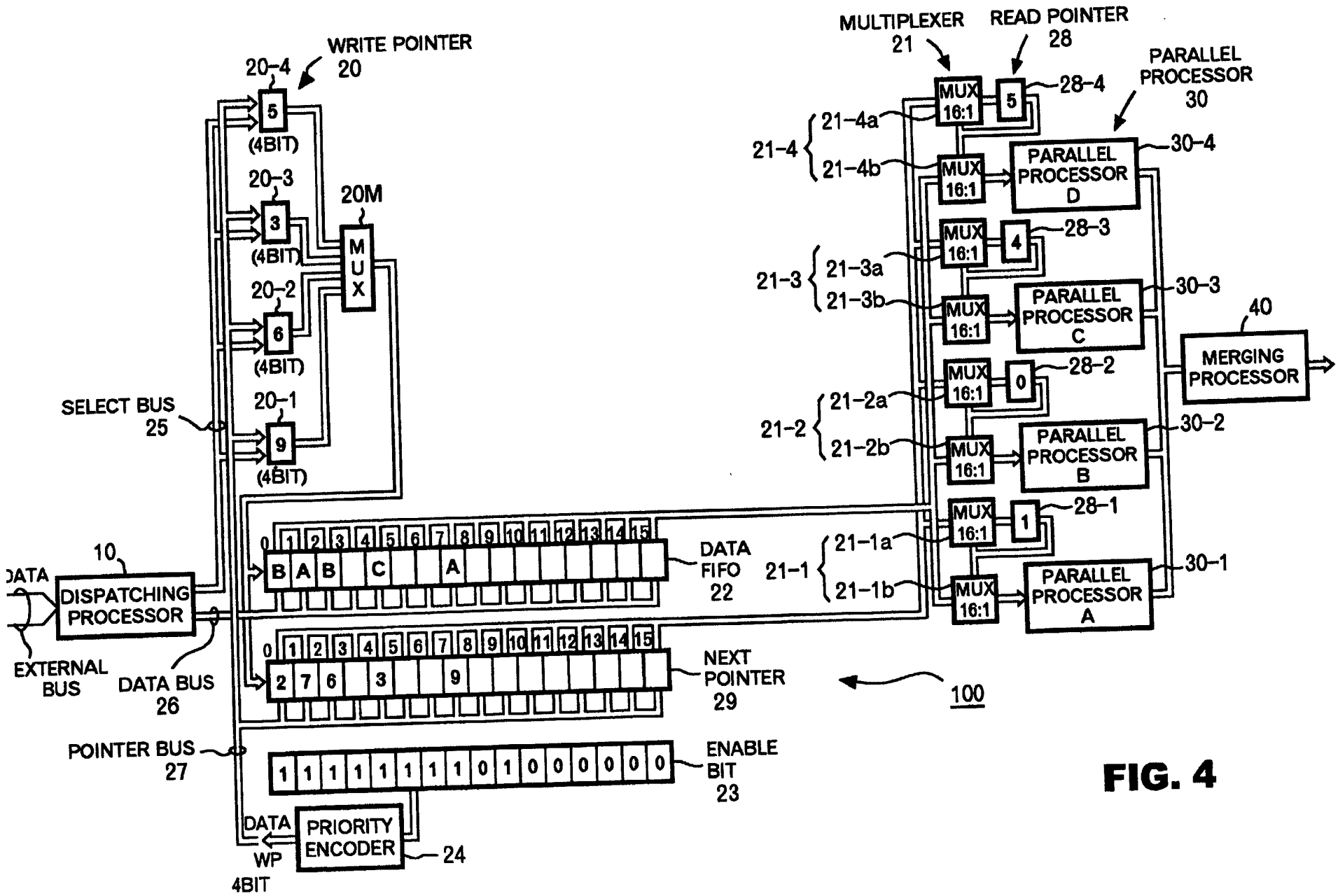

FIG. 4

Patent Application Publication

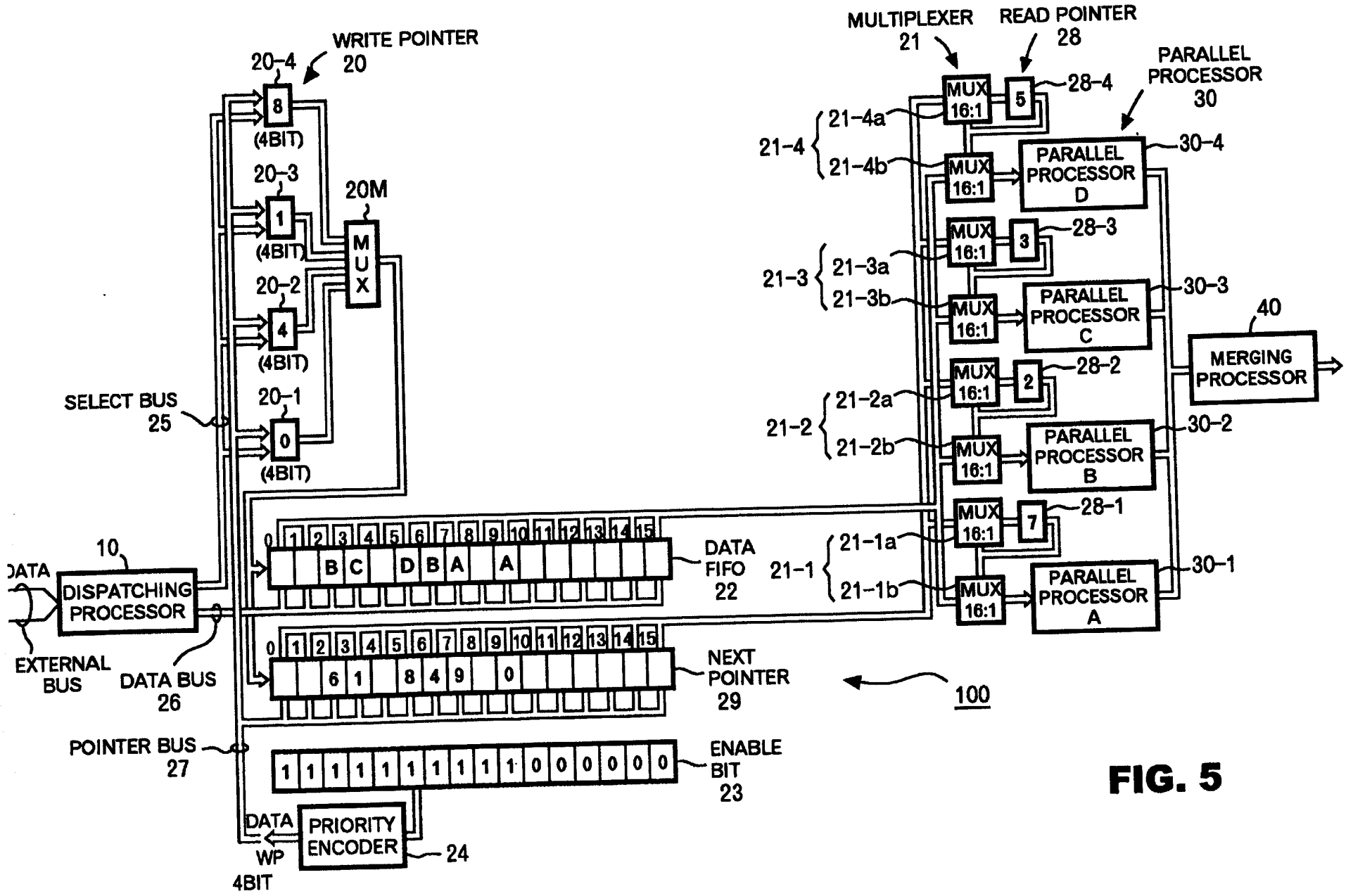

FIG. 5

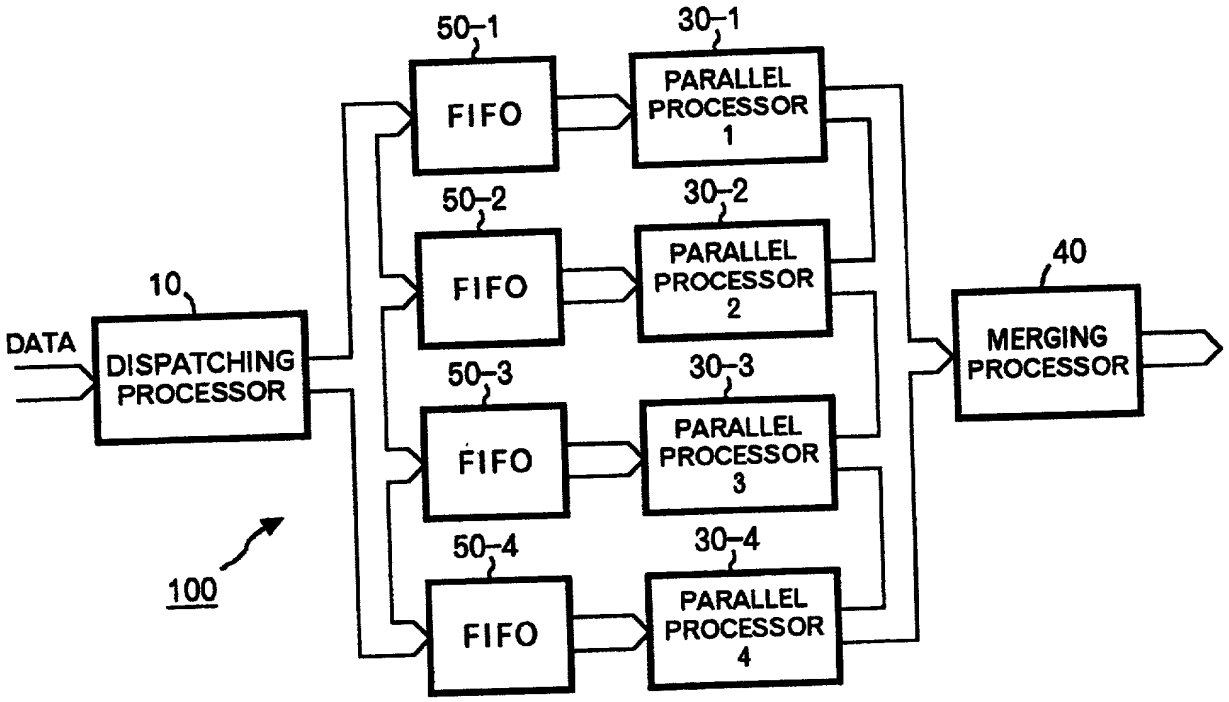

FIG. 6

	CASE(a)	CASE(b)	CASE(c)
PARALLEL PROCESSOR 1	1	2	2
PARALLEL PROCESSOR 2	3	1	8
PARALLEL PROCESSOR 3	2	5	1
PARALLEL PROCESSOR 4	1	1	3

FIG. 7

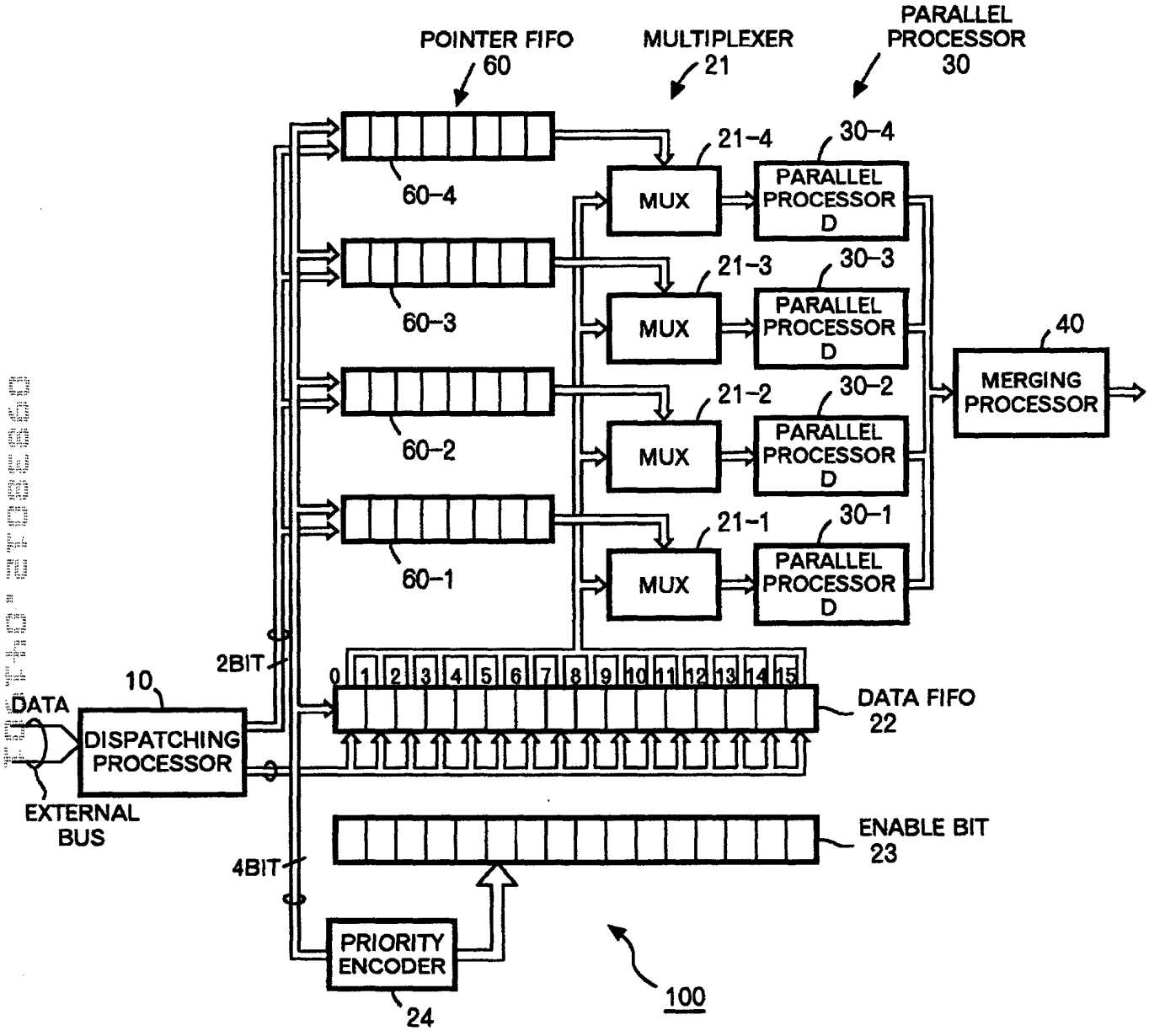
POINTER FIFO
60
MULTIPLEXER
21
PARALLEL
PROCESSOR
30
60-4
60-3
60-2
60-1
21-4
21-3
21-2
21-1
30-4
30-3
30-2
30-1
MUX
PARALLEL
PROCESSOR
D
40
MERGING
PROCESSOR
2BIT
10
DATA
DISPATCHING
PROCESSOR
EXTERNAL
BUS
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
DATA FIFO
22
ENABLE BIT
23
4BIT
PRIORITY
ENCODER
24
100

FIG. 8